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10/552,364	06/09/2006	Christopher Julian Travis	GRP-0142	8785

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EXAMINER	
GANNON, LEVI	

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2817	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,364	TRAVIS, CHRISTOPHER JULIAN	
	Examiner	Art Unit	
	LEVI GANNON	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-90* is/are pending in the application.

4a) Of the above claim(s) *23-54 and 59-86* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-22,55-58 and 87-90* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/28/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Note: While claim 86 has been withdrawn, the claim will ultimately need to be amended to fix the improper multiple dependent form or be cancelled from the claim listing. See MPEP § 608.01(n).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10, 12-22, 55-58, and 87-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wunner et al. (hereinafter "Wunner") (US Patent 6,674,332; reference of record) in view of Eriksson (US Patent 5,986,512; reference disclosed by Applicant).

Regarding claim 1, Wunner discloses a method (Note figures 4 and 5) of establishing an output clock signal (output of 533 and 212E in figure 5) on a basis of an input timing reference (Input Ref 205), said method comprising: attenuating jitter (using loop filter 432) of said input timing reference to produce a control signal (216"), providing at least one intermediate clock signal (output of divider 212C) on a basis of said control signal, at least one of said intermediate clock signals (213 and output of

divider 212C) being justified to a local clock (provided by crystal 242), and providing said output clock signal (output of 533 and 212E in figure 5) on a basis of said at least one intermediate clock signal (213 and output of divider 212C) by attenuating jitter (using loop filter 532) of said at least one intermediate clock signal (213 and output of divider 212C).

Wunner does not teach the intermediate clock signal being spectrum controlled.

Eriksson teaches a well known method of spread spectrum control (note figure 1) including the use of a dithering signal generator (44) and noise shaping delta-sigma modulator (38). This well known method of spread spectrum control is used for setting a value for a frequency divider and for the obvious spectrum control.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to add the spread spectrum control of Eriksson to the output clock signal generator (figures 4 and 5) of Wunner because such a modification would provide the benefit of providing a frequency divider value to frequency divider 212C and providing the output clock signal generator of Wunner with spectrum control.

In terms of claim 2, Wunner teaches at least a part of the jitter of said at least one intermediate clock signal (213 and output of divider 212C) comprises justification jitter originating from said justification to said local clock (provided by crystal 242).

As for claim 3, Wunner teaches the justification and spectrum control being performed numerically (By way of controlling oscillator 232" frequency and divider 212C). Also, note use of digital circuitry in col. 7, lines 49-51.

As for claim 4, Wunner teaches the attenuation of jitter of said input timing reference (205) being performed by using a filter (in filter 432) but does not expressly teach the filter being a low-pass filter.

However, it is well known to those of ordinary skill in the art to use low pass filters as the loop filter in a phase locked loop for removing unwanted high frequency signals from the loop.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the filter of Wunner with a low pass filter because such a modification would have provided the benefit of removing unwanted high frequency signals from the loop.

In terms of claim 5, Wunner teaches the justification being performed by means of a number-controlled oscillator (comprising oscillator 232" and frequency divider 212C).

Regarding claim 6, Wunner a control input (f216") of said number-controlled oscillator (comprising oscillator 232" and frequency divider 212C) comprises a period control input.

Regarding claims 7 and 8, Wunner modified by Eriksson teaches the spectrum control comprising dithering or noise shaping. Note col. 4, lines 47-52.

As for claims 9 and 10, Wunner teaches the local clock being derived from a stable crystal reference clock (242).

Regarding claim 12, Wunner discloses the attenuation of jitter of said input timing reference (205) is performed by means of a first block (figure 4), which preferably

comprises a time-locked loop (see figure 4), with reference to a stable reference clock (crystal 242).

As for claim 13, Wunner teaches at least a part of said justification jitter (derived by oscillator 232" and divider 212C) being biased into a higher frequency band (jitter may be biased into whatever frequency band is determined by oscillator 232" and divider 212C).

In terms of claim 14, Wunner discloses the justification jitter being low-pass filtered by means of a second block (figure 5), which preferably comprises a phase-locked loop (note figure 5).

As for claim 15, Wunner teaches the second block (figure) producing a multiplied clock (output of 533).

Regarding claim 16, Wunner teaches the second block (figure 5) further produces a frame signal (210), said frame signal (210) being established by means of frequency division (with 212E) of said multiplied clock (output of 533).

Regarding claim 17, Wunner teaches intermediate clock signals (213 and output of 212C) is established by means of at least one numeric stage (figure 4).

As for claim 18, Wunner teaches the attenuating jitter of said at least one intermediate clock signal (213 and output of 212C) is performed by means of at least one analog stage (figure 5).

In terms of claim 19, Wunner teaches the analog stage (figure 5) is adapted for attenuating jitter partly or mainly originating from said at least one numeric stage (figure 4).

As for claim 20, Wunner discloses the intermediate clock signals (IC) being justified to a corresponding local clock (from crystal 242) and justification jitter associated with said justification to said local clock is spectrum controlled (with chosen frequency of oscillator 232" and frequency divider 212C).

As for claim 21, Wunner teaches the intermediate clock signals (213 and output of 212C) comprising an intermediate event clock component (213) and an intermediate framing component (output of 212C), said intermediate framing being established on a basis of said intermediate event clock by means of frequency division (with 212C).

In terms of claim 22, Wunner discloses the output clock signal (210 and output of 533) comprises an output event clock component (output of 533) and an output framing component (210), said output framing being established on the basis of said output event clock by means of frequency division (with 212E).

In terms of claim 55, Wunner teaches a clock synchronizer (Wunner synchronizes input 205 and output 210) for establishment of an output clock signal (210 and output of 533) according to claim 1.

As for claim 56, Wunner teaches a number-controlled oscillator (comprising oscillator 232" and frequency divider 212C).

In terms of claim 57, Wunner discloses a circuit (figure 4) for attenuating jitter of an input timing reference (205), said circuit comprising a number-controlled oscillator (comprising oscillator 232" and frequency divider 212C) adapted for establishment of an intermediate clock signal (213 and output of 212C) on the basis of said input timing reference (205).

Regarding claim 58, Wunner teaches jitter filtering means (figure 5) adapted for providing said output clock signal (210 and output of 533) on the basis of said intermediate clock signal (213 and output of 212C).

As for claim 87, Wunner teaches the second block (figure 5) comprising an asynchrony detector (531).

In terms of claims 88-90, Wunner teaches the output clock signal (210 and output of 533) being phase, frequency, and frequency ratio locked to the input timing reference (205).

Allowable Subject Matter

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The best art of record, Wunner, taken alone or in combination of other references fails to teach or suggest "... *said local clock is derived from said output clock signal*.", as set forth in claim 11.

Response to Arguments

Applicant's arguments, see top of page 18 dealing with spectrum control and middle of page 18 dealing with low pass filtering, filed 02/25/2008, with respect to the rejection(s) of claim(s) 1 and 4 under 35 U.S.C. 102(b) have been fully considered and

are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Eriksson, as stated above.

Applicant's arguments, see top of page 20, filed 02/25/2008, with respect to the rejection(s) of claim(s) 7 and 8 under 35 U.S.C. 103(a) have been fully considered and **are persuasive**. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Eriksson, as stated above.

Applicant's arguments, see bottom of page 19 and top of page 20, filed 02/25/2008, with respect to claims 1 and 11 rejected under U.S.C. 102(b) over Wang have been fully considered and **are persuasive**. The rejection of claims 1 and 11 has been withdrawn.

The following Applicant's arguments filed 02/25/2008 have been fully considered but they **are not persuasive**.

a) Regarding claim 1, Applicant states (pg. 16-17) that Wunner does not teach the intermediate clock signal being justified to a local clock. The Applicant also gives various definitions for "justification". The definition at the top of page 17 reads "The movement and alignment of data with respect to a fixed reference, such as a clock or frame alignment signal."

According to this definition Wunner teaches the intermediate clock signal (output of divider 212C) being justified to a local clock (provided by crystal 242). The data output from divider 212C is aligned with respect to the reference signal provided by crystal 242.

b) Applicant also states (bottom of page 17) "Furthermore, the asynchronicity of the above discussed justification leads to jitter. Wunner does not teach or suggest introduced jitter or attenuation of said jitter..." However, claims 1 and 4 teach the jitter being attenuated by the filter FLF in order to produce the control signal 103 for the oscillator. The asynchronicity of the justification does not produce the jitter, the jitter is already present in the timing reference TR. There is an inherent jitter present in the input reference 205 of Wunner also.

c) With regards to claim 3 (and also claims 5, 56, and 57), Applicant argues (page 18) that the justification and spectrum control are not numerical due to the lack of a numerically controlled oscillator. This argument is not persuasive because the oscillator of Wunner is a digital oscillator that would be numerically controlled. Note col. 7, lines 49-51.

d) Regarding claim 6, Applicant notes that Wunner does not teach a period control element. This argument is not persuasive because if the oscillator's frequency is controlled, then the oscillator's period is inherently controlled due to the inherent inverse relationship between frequency and period.

e) With reference to claim 12, Applicant states that the first loop is not a time locked loop, but merely a phase locked loop. This argument is not persuasive because

the phase locked loop of Wunner is both phase locked and frequency locked. Note col. 2, lines 30-33.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEVI GANNON whose telephone number is (571)272-7971. The examiner can normally be reached on Monday-Friday 9:30AM-6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LG
06/05/08

/Robert Pascal/
Supervisory Patent Examiner, Art Unit 2817